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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,401	KIM, DU-YEUL	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-16* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/824,401 has a total of 16 claims pending in the application, there are 3 independent claims and 13 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by MPEP § 201.14(c), acknowledgment is made of Applicant's claim for priority based on an application filed in the Korean Intellectual.Property Office on June 5, 2003.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statement dated October 6, 2005 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Pipeline Memory Device Employing a Data Fetching Method That Can Be Operated at Higher Frequencies."

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The subject matter in question is the multiplexer disclosed in claims 2-3 and 15. Paragraph 0021, lines 2-8 of Applicant's specification is the only

place within Applicant's detailed description that describes the multiplexer in which it is stated that "The multiplexer 520 generates the second pipeline control signal SRP by multiplexing the first pipeline control signal FRP and the output of the edge trigger delay circuit 510." From this section of Applicant's specification Examiner is unable to clearly discern whether Applicant's multiplexer functions as a multiplexer used commonly in the computer architecture arts or a multiplexer used commonly in the communication arts. In the computer architecture arts a multiplexer **chooses** which of multiple inputs should be the singular output based on select lines. The most basic multiplexer in the computer architecture arts would have 2 inputs, 1 select line, and 1 output, thus giving the system a total of 3 unique inputs and 1 unique output. However, Applicant's multiplexer has only 2 unique inputs (FRP and the delayed PCLK) and therefore it cannot properly function as a typical multiplexer found in the computer architecture arts. Conversely, a multiplexer in the communication arts **combines** multiple inputs to create a singular output. However, if Applicant's multiplexer functions as a typical multiplexer found in the communication arts the specification does not disclose what form of multiplexing occurs (i.e. code-division multiplexing, frequency-division multiplexing, time-division multiplexing, wavelength-division multiplexing, etc.); information necessary in order for one of ordinary skill in the art to ascertain how the claimed invention functions. Nonetheless, for the purposes of this instant office action Examiner will interpret the multiplexer to function as a typical multiplexer found in the computer architecture arts.

Appropriate correction is required.

Claims

7. **Claim 16** objected to because of the following informalities: On line 2 the phrase "utilizing NAND gate" should read "utilizing a NAND gate."

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. **Claims 2-3 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The subject matter in question is the multiplexer disclosed in claims 2-3 and 15. Paragraph 0021, lines 2-8 of Applicant's specification is the only place within Applicant's detailed description that describes the multiplexer in which it is stated that "The multiplexer 520 generates the second pipeline control signal SRP by multiplexing the first pipeline control signal FRP and the output of the edge trigger delay circuit 510." From this section of Applicant's specification Examiner is unable to clearly discern whether Applicant's multiplexer functions as a multiplexer used commonly in the computer architecture arts or a

multiplexer used commonly in the communication arts. In the computer architecture arts a multiplexer **chooses** which of multiple inputs should be the singular output based on select lines. The most basic multiplexer in the computer architecture arts would have 2 inputs, 1 select line, and 1 output, thus giving the system a total of 3 unique inputs and 1 unique output. However, Applicant's multiplexer has only 2 unique inputs (FRP and the delayed PCLK) and therefore it cannot properly function as a typical multiplexer found in the computer architecture arts. Conversely, a multiplexer in the communication arts **combines** multiple inputs to create a singular output. However, if Applicant's multiplexer functions as a typical multiplexer found in the communication arts the specification does not disclose what form of multiplexing occurs (i.e. code-division multiplexing, frequency-division multiplexing, time-division multiplexing, wavelength-division multiplexing, etc.); information necessary in order for one of ordinary skill in the art to ascertain how the claimed invention functions. Nonetheless, for the purposes of this instant office action Examiner will interpret the multiplexer to function as a typical multiplexer found in the computer architecture arts.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3 and 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. **As per claim 3**, the claim recites the limitation "the first and second edge trigger delay circuits" in lines 1-2. There is insufficient antecedent basis for this limitation in the

claim. Applicant may consider amending the claim to read simply "the first edge trigger delay circuit."

13. **As per claim 10**, the claim discloses that the first and the second control signal are driven by a clock signal (the "a" implying a singular clock). However, Applicant's specification and drawings imply that the first and second control signals are actually driven by two separate internal clock signals (FRP and SRP respectively). Alternatively, these two internal clock signals are driven by a singular external clock signal (CLK). Thus, it would follow that the external clock signal (CLK) would inherently drive both the first and the second control signal. Accordingly, Examiner will interpret "a clock signal" as recited in claim to refer to the external clock signal (CLK) found in Applicant's specification.

14. **As per claim 11**, due to the aforementioned interpretation of claim 10, Examiner will consequently interpret "the clock signal is an internal clock signal" to be "the clock signal is an external clock signal" because the two separate clock signals (FRP and SRP) are internal while the singular clock signal (CLK) is external.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1 and 6-14 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's "Description of the Related Art" appearing in Applicant's specification and drawings, hereafter referred to as "Applicant's admitted prior art" in view of Lee (U.S. Patent 6,564,287).

17. **As per claim 1**, Applicant's admitted prior art discloses a pipeline memory device comprising:

a plurality of memory cells that store data (paragraph 0004, lines 3-5; Fig. 1, elements 21 and 22);

a data transfer path on which the data is transferred (paragraph 0005, lines 6-9; Fig. 1, element 32); *It should be noted that "data pipeline stage" is analogous to "data transfer path."*

a first pipeline stage which latches the data on the data transfer path in response to the first pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 26);

a second pipeline stage which latches the data latched by the first pipeline stage in response to the second pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 28);

and a third pipeline stage which outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal (paragraph 0005, lines 9-13; Fig. 1, elements 30 and 34). *It should be noted that "data output buffer" is analogous to "data output pad."*

Applicant's prior art does not expressly disclose a data fetching control circuit which generates:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal;

and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal.

Lee discloses a data fetching control circuit which generates:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal (col. 3, lines 22-28; Fig. 3, elements p3 and CLK); *It should be noted that "pipeline control signal p3" is analogous to "first pipeline control signal" and "clock signal CLK" is analogous to "first clock signal."*

and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3). *It should be noted that "pipeline control signal p2" is analogous to "second pipeline control signal." It should also be noted that p3 is* ***both*** *a control signal* ***and*** *a clock signal. p3 is merely a buffered version of "clock signal CLK." p3 also acts as a control signal which is sent to from the "pipeline control signal generation circuit" to the "pipeline circuit" (Fig. 1, elements 28 and 30). Therefore, p3 is analogous to* ***both*** *a "second clock signal"* ***and*** *a "first pipeline control signal." Since p2 is created in response to p3 it follows that Lee discloses "a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal."*

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first and second stages of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 1.

18. **As per claim 6**, Applicant's admitted prior art discloses a data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path (paragraph 0005, lines 6-9; Fig. 1, element 32);

latching the data to a first pipeline stage on the transfer path in response to the first pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 26);

latching the data to a second pipeline stage on the transfer path in response to the second pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 28);

and outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal (paragraph 0005, lines 9-13; Fig. 1, elements 30 and 34). *Please see citation notes for similar limitations in claim 1 above.*

Applicant's admitted prior art does not expressly disclose generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal.

Lee discloses generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal (col. 3, lines 22-28; Fig. 3, elements p3 and CLK);

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3). *Please see citation notes for similar limitations in claim 1 above.*

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first and second stages of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 6.

19. **As per claim 7**, Lee discloses a point of activation of the second pipeline control signal is determined depending on a point of activation of the first pipeline control signal (col. 3, lines 34-37; Fig. 6, time diagrams for p3 and p2). *It should be noted that since p2 directly dependent on p3 it is inherently required p2 is activated at some point after p3 has been activated. The time diagrams from Fig. 6 confirm that p2 is activated after p3 has been activated.*

20. **As per claim 8**, Lee discloses the second pipeline control signal is activated when the first pipeline control signal is inactive (Fig. 6, time diagrams for p3 and p2). *It should be noted that when looking at Fig. 6 it is clear that p2 goes high (active) for the first time after p3 goes low (inactive) for the first time.*

21. **As per claim 9**, Applicant's admitted prior art discloses an apparatus comprising:

at least one memory cell (paragraph 0004, lines 3-5; Fig. 1, element 21);

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal (paragraph 0005; Fig. 1, elements 21, 24, and 26);

and a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by a second control signal (paragraph 0005, lines 9-13; Fig. 1, elements 26-28).

Applicant's admitted prior art does not expressly disclose the second pipeline stage is driven by the first control signal and a second control signal.

Lee discloses a second control signal driven by a first control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3).

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first second stage of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 9.

22. **As per claim 10**, Lee discloses the first control signal and the second control signal are driven by a clock signal (col. 3, lines 22-28 and 34-37; Fig. 3, elements p3, p2, and CLK). *It should be noted that CLK drives p3 and p3 in turn drives p2, therefore, CLK inherently drives both p3 and p2.*

23. **As per claim 11**, Lee discloses the clock signal is an external clock signal (col. 3, lines 25). *Please note the 112, 2nd paragraph rejection to claim 11 above. It should also be noted that "clock signal CLK applied form the external source" is analogous to "external clock signal."*

24. **As per claim 12**, Lee discloses the first control signal is delayed from the clock signal by a first delay (Fig. 6, time diagrams for p3 and CLK); *It should be noted that the "first delay" between CLK and p3 is taken from a falling edge of CLK until the next full rising edge of p3.*

and the second control signal is delayed from the clock signal by a second delay (Fig. 6, time diagrams for p2 and CLK). *It should be noted that the "second delay" between CLK and p2 is taken from a falling edge of CLK until the next full rising edge of p2.*

25. **As per claim 13**, Lee discloses the first delay is larger than the second delay Fig. 6, time diagrams for p3, p2, and CLK). *It should be noted that time (i.e. delay) from a falling edge of CLK until the next full rising edge of p3 is larger than the time from a falling edge of CLK until the next full rising edge of p2.*

26. **As per claim 14**, Lee discloses the first control signal and the second control signal are never in an active state at the same time (Fig. 6, time diagrams for p3 and p2). *It should be noted that p3 is only high (active) when p2 is low (inactive) and vice versa.*

27. Claims 2-3 and 15 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lee as applied to claims 1 and 9 above, and in further view of Paul et al. (U.S. Patent 6,629,226).

28. **As per claim 2**, Applicant's admitted prior art/Lee discloses a first edge trigger delay circuit which receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal (Applicant's admitted prior art,

paragraph 0009, lines 1-5); *It should be noted that "internal clock signal PCLK" is analogous to "first clock signal."*

Applicant's admitted prior art/Lee does not expressly disclose a multiplexer which receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal.

Paul discloses a multiplexer which receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal (col. 5, lines 45-51; Fig. 5, elements 164, 165, ADDRESS (@SYSCLK), and CTR). *It should be noted that "ADDRESS (@SYSCLK)" is analogous to "second clock signal" and "CTR" is analogous to "first pipeline control signal." It should also be noted that the output of "MUX 164" is analogous to the "second pipeline control signal."*

Applicant's admitted prior art/Lee and Paul are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Paul's MUX which uses a control signal and clock signal to create another control signal to drive a pipeline stage within Applicant's admitted prior art/Lee's the pipeline memory device.

The motivation for doing so would have been to eliminate synchronizing problems with configuration dependent latencies (Paul, col. 2, lines 45-46).

Therefore, it would have been obvious to combine Applicant's admitted prior art/Lee and Paul for the benefit of obtaining the invention as specified in claim 2.

29. **As per claim 3**, Applicant's admitted prior art discloses the first and second edge trigger delay circuits compromise an even number of inverters in a chain (paragraph 0009, line 1; Fig. 3, element 300).

30. **As per claim 15**, Paul discloses the second pipeline stage is driven by the first control signal and the second control signal utilizing a multiplexer (col. 5, lines 48-51; Fig. 5, elements 164, 165, and CTR). *Please see citation notes for claim 2 above.*

31. Claim 16 is rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lee as applied to claim 9 above, and in further view of Shinozaki (U.S. Patent 6,084,802).

32. Applicant's admitted prior art/Lee discloses all the limitations of claim 16 except the second pipeline stage is driven by the first control signal and the second control signal utilizing NAND gate.

Shinozaki discloses the second pipeline stage is driven by the first control signal and the second control signal utilizing NAND gate (col. 8, lines 42-47; Fig. 8, elements 42, 43, and Hz). *It should be noted that "Hz" is analogous to "first control signal" and "drive signal 42" is analogous to "second control signal."*

Applicant's admitted prior art/Lee and Shinozaki are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Shinozaki's NAND gate with two control signals used to drive the second stage of the pipe-line circuit within Applicant's admitted prior art/Lee's second stages of the pipeline memory device.

The motivation for doing so would have been to provide a semiconductor memory device which can keep the timing of an output signal from an output circuit at a predetermined phase difference to a supplied external clock in accordance with the period of the external clock, and can guarantee the proper operation of internal circuits with a pipe-line structure (Shinozaki, col. 2, lines 3-9).

Therefore, it would have been obvious to combine Applicant's admitted prior art/Lee and Shinozaki for the benefit of obtaining the invention as specified in claim 16.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

33. **Claims 4 and 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

34. The primary reasons for allowance of **claims 4 and 5** in the instant application is the combination with the inclusion in claim 4 that "**a first edge trigger delay circuit that receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal; a second edge trigger delay circuit that receives the second clock signal for generating the second pipeline control signal; a first inverter that inverts the first pipeline control signal; a NAND gate**

that receives the output of the first inverter and the second edge trigger delay circuit; and a second inverter that inverts the output of the NAND gate to output the second pipeline control signal." The prior art of record neither anticipates nor renders obvious the above recited combination.

35. If Applicant should choose to rewrite the independent claims to include the limitations recited in either one of **claims 4 and 5**, the applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

36. As allowable subject matter has been indicated, Applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Claims Rejected in the Application

37. Per the instant office action, **claims 1-3 and 6-16** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,192,005 discloses a clock control signal and output enable signal generator in semiconductor memory device.

2. U.S. Patent 6,266,750 discloses a method and apparatus for implementing a variable length pipeline in a packet-driven memory control system.

3. U.S. Patent 6,351,433 discloses a semiconductor memory device employing pipeline operation with reduced power consumption.

4. U.S. Patent 6,363,465 discloses a synchronous data transfer system and method with successive stage control allowing two more stages to simultaneous transfer

5. U.S. Patent 6,427,197 discloses a semiconductor memory device operating in synchronization with a clock signal for high-speed data write and data read operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
April 13, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER